Intel® 31154 133MHz PCI Bridge Evaluation Board

User's Guide

January 2005

Order Number: 278849-002

Contents

Figures

Tables

Revision History

Date	Revision	Description
January 2005	002	Initial Public Release
November 2003	001	Initial Preliminary Version

Introduction 1

This document describes the 31154 133MHz PCI Bridge (also called 31154 Bridge) Evaluation Board.

1.1 Overview

The 31154 Bridge is a PCI expansion board that is used to evaluate the operation of the 31154 Bridge. The 31154 Bridge can be used to perform the following functions:

- Develop initialization code to configure the 31154 Bridge and associated logic and devices on the local PCI bus as a intelligent controller.
- Evaluate the operation of the 31154 Bridge with a variety of PCI devices configured in an intelligent subsystem.
- Build and evaluate a system.
- Testing of the 31154 Bridge feature set.

1.2 Features

The 31154 Bridge has the following features:

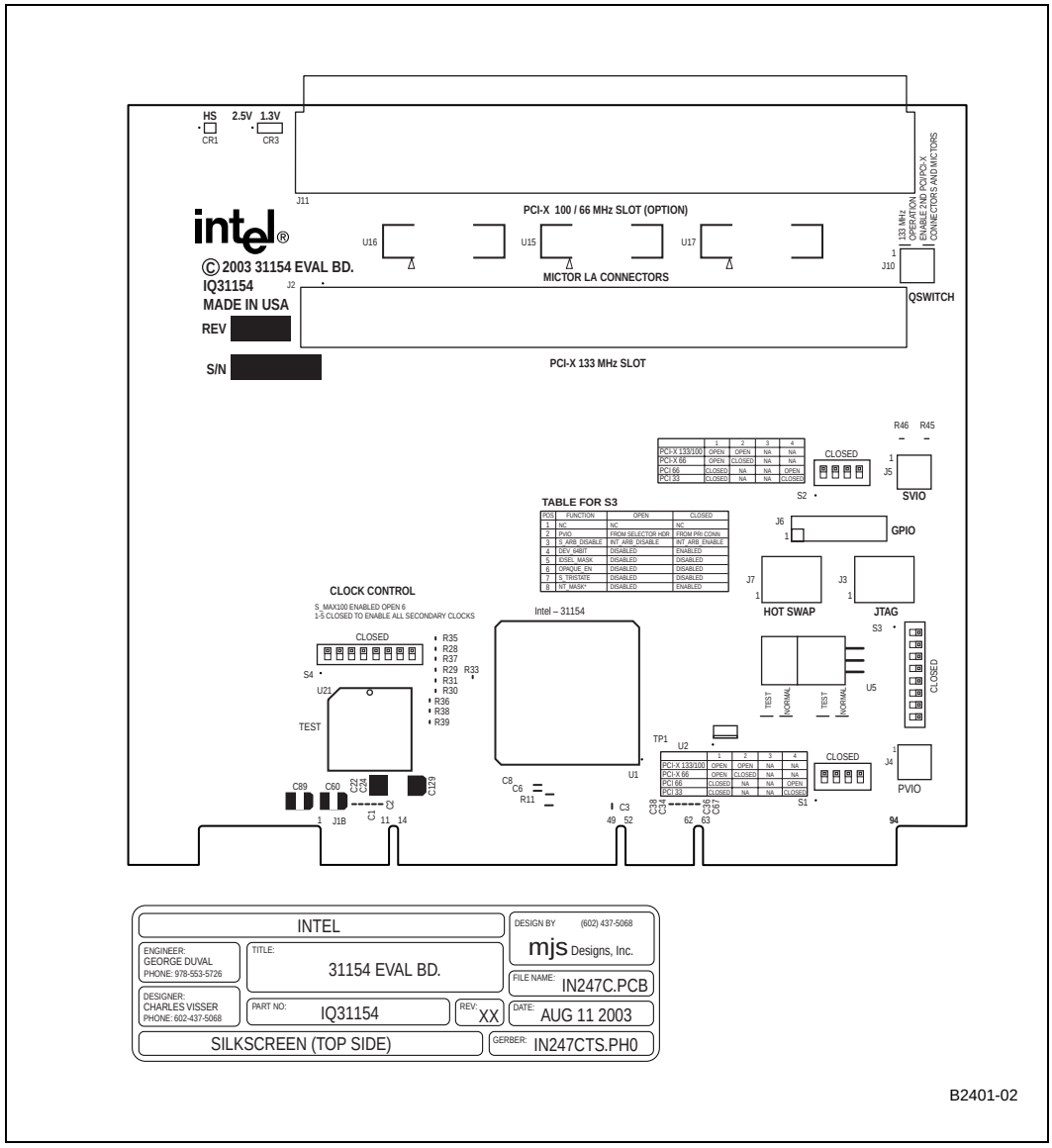
- Complies fully with the protocol and electrical standards of Revision 2.3 of the *PCI Local Bus Specification and PCI-X 1.0 rev A, Bridge Architecture.*
- Includes a 31154 Bridge "transparent" PCI-X Enhanced PCI-to-PCI Bridge that provides bridging between two processor domains.
- Includes a host PCI interface that plugs into any 3-V PCI option card slot.
- Provides a PCI-X 133 MHz slot, PCI-X100/66 MHz slot, and three MICTOR LA connectors for logic analyzer interfacing.
- Support, Product information, and Documentation is available on the Intel Developer’s web site.

1.3 Major Components

The major components for the 31154 Bridge include:

- J11 is the PCI-X 100/66 MHz card slot. J2 is the PCI-X 133 MHz card slot.
- MICTOR connectors U15 and U17 provide test points for the 64-bit S_AD signals. MICTOR connector U16 provides test points for the PCI control, CBE and REQ/GNT signals.
- J3 is the JTAG connector. J6 provides access to the General Purpose I/O pins. S1, S2, S3, & S4 are option switches. Additional option jumpers are described in the following sections.
- U21 is a Test socket, providing access to the PCI control signals.

Figure 1. Mainboard Components[1]



1.4 Dip switches[1]

The 31154 Bridge uses a combination of switches and jumpers to control the various configuration options. The following sections describe these controls.

1. All switches are shipped in the CLOSED position.

1.4.1 Switch Settings

Table 1, Table 2, and Table 3 describe the function of the 31154 Bridge Evaluation Board switches. The switches should be set before powering up the system. Figure 1 shows the Evaluation board switches.

Note: When a switch is ON, it is Closed.

Table 1. DIP Switch Operation, PCI-X and PCI Clock Frequency

Switch	Function	Pos 1	Pos 2	Pos 3	Pos 4
S1	Selects Primary PCI-X 133/100 MHz	Open	Open	N/A	N/A[a]
S1	Selects Primary PCI-X 66 MHz	Open	Closed	N/A	N/A[a.]
S1	Selects Primary PCI 66 MHz	Closed	N/A	N/A	Open
S1	Selects Primary PCI 33 MHz	Closed	N/A	N/A	Closed
S2[b]	Selects Secondary PCI-X 133/100 MHz	Open	Open	N/A	N/A[a.]
S2	Selects Secondary PCI-X 66 MHz	Open	Closed	N/A	N/A[a.]
S2	Selects Secondary PCI 66 MHz	Closed	N/A	N/A	Open
S2	Selects Secondary PCI 33 MHz	Closed	N/A	N/A	Closed

a. For A0 Silicon, Pos 4 must be Closed for PCI-X operation.
b. S2 is dependent on S4 settings. See Table 3.

Table 2. DIP Switch Operation, Hardware Option Straps

Switch	Position	Function	Open	Closed
S3	1	NC	NC	NC
S3	2	PVIO source	From Selector Header	***From Primary Conn***
S3	3	S_ARB_DISABLE#	INT ARB Disabled	***INT ARB Enabled***
S3	4	DEV_64BIT#	***Disabled***	Enabled
S3	5	IDSEL_MASK	Enabled	***Disabled***
S3	6	OPAQUE_EN	Enabled	***Disabled***
S3	7	S_TRISTATE	Enabled	***Disabled***
S3	8	NT_MASK#	***Disabled***	Enabled

Note: ***BOLD*** settings are Defaults.

Table 3. DIP Switch Operation, Clock Source

Switch	Function	Pos 6	Pos 5	Pos 4 CLKEN3	Pos 3 CLKEN2	Pos 2 CLKEN1	Pos 1 CLKEN0
S4	S_CLKO 8	N/A	N/A	Open	Closed	Closed	Closed
S4	S_CLKO 7	N/A	N/A	Closed	Open	Open	Open
S4	S_CLKO 6	N/A	N/A	Closed	Open	Open	Closed
S4	S_CLKO 5	N/A	N/A	Closed	Open	Closed	Open
S4	S_CLKO 4	N/A	N/A	Closed	Open	Closed	Closed
S4	S_CLKO 3	N/A	N/A	Closed	Closed	Open	Open
S4	S_CLKO 2	N/A	N/A	Closed	Closed	Open	Closed
S4	S_CLKO 1	N/A	N/A	Closed	Closed	Closed	Open
S4	S_CLKO 0	N/A	N/A	Closed	Closed	Closed	Closed
S4	100 MHz EN	Open	N/A	N/A	N/A	N/A	N/A
S4	133 MHz EN	Closed	N/A	N/A	N/A	N/A	N/A
S4	Global CLK EN	N/A	Open	N/A	N/A	N/A	N/A

Note: S4 Positions 7 and 8 are no connects (NC).

1.5 Jumpers

In addition to the DIP switches, the 31154 Bridge provides stake-pin jumpers for selecting special features. The jumpers can be used for debugging and for evaluating special features. Tables 1–4 through 1-11 show the configuration jumpers and the jumper function. Figure 1 shows the 31154 Evaluation Board jumpers.

Table 4. Jumper Connections, JTAG Port

Jumper	Function	Default
J3-2,1	TCK Test Clock	***Not Installed***
J3-4,3	TDO Test Data Out	***Not Installed***
J3-6,5	TDI Test Data In	***Not Installed***
J3-8,7	TMS Test Mode Select	***Not Installed***
J3-10,9	TRST# Test Reset	***Not Installed***
J3-1,3,5,7,9	GND	
J3-11,12	NC	

Table 5. Jumper Connections, General Purpose I/O, GPIO Header

Jumper	Function	Default
J6-1,2	GPIO(7)	***Not Installed***
J6-3,4	GPIO(6)	***Not Installed***
J6-5,6	GPIO(5)	***Not Installed***
J6-7,8	GPIO(4)	***Not Installed***
J6-9,10	GPIO(3)	***Not Installed***
J6-11,12	GPIO(2)	***Not Installed***
J6-13,14	GPIO(1)	***Not Installed***
J6-15,16	GPIO(0)	***Not Installed***
J6-2,4,6,8,10,12,14,16	GND	

Table 6. Jumper Connections, Compact PCI HOT SWAP Header

Jumper	Function	Position	Default
J7-1,2	HS_ENUM#	5	***Not Installed***
J7-3,4	HS_LSTAT	4	***Installed*** = ejector handle closed
J7-5,6	HS_SM	3	***Installed***
J7-7,8	HS_FREQ(1)	2	***Installed***
J7-9,10	HS_FREQ(0)	1	***Installed***
J7-2,4,6,8,10	GND		
J7-11,12	NC		

For Non-Hot Swap Support, Install Jumpers in J7 Positions 1, 2, 3, & 4.

Table 7. Jumper Connections, PVIO Voltage Clamp

Function	Installed	Not Installed
PVIO 3.3V	J4-2 to J4-3	J4-1
PVIO 5V	J4-1 to J4-2	J4-3
PVIO From Edge Connector	***N/A***	***J4-1,2,3***

Selection for the Primary Bus PCI Universal I/O Voltage Reference is provided. J4 jumpers connect **PVIO** to either 3.3V or 5V. To clamp for 3.3V **all** option cards on the local bus must be 3-volt options.

Note: Normal Operation, J4 is Open, with S3 Pos 2 Closed.

Table 8. Jumper Connections, SVIO Voltage Clamp

Function	Installed	Not Installed
SVIO 3.3V	***J5-2 to J5-3***	***J5-1***
SVIO 5V	J5-1 to J5-2	J5-3

Selection for the Secondary Bus PCI Universal I/O Voltage Reference is provided. J5 jumpers connect **SVIO** to either 3.3V or 5V. To clamp for 3.3V **all** option cards on the local bus must be 3-volt options.

Note: ***BOLD*** settings are Defaults.

Table 9. Jumper Connections, QSWITCH EN Header

Function	Installed	Not Installed
For 133 MHz Operation	J10-1 to J10-2	J10-3
Enables 2nd PCI/PCI-X Connector & MICTOR LA Connectors	J10-2 to J10-3	J10-1

Note: J10 straps the QSWITCHEN# line.

Installation 2

This chapter provides information about the 31154 Bridge specifications and the hardware and software requirements for using the 31154 Bridge. It also describes how to install the 31154 Bridge.

2.1 Specifications

The physical and power specifications for the 31154 Bridge are as follows:

Dimensions:

- Height: 16.5 cm (6.5 in)
- Width: 17.8 cm (7.0 in)

Power Requirements:

- 5V 2A Max
- 3.3V 2.5A Max
- On Board 5 volt regulator for Core 1.3V VCC1_3: 0.85 Watts (Maximum)

2.2 Hardware Requirements

The following equipment is required to use the 31154 Bridge:

- A computer system equipped with PCI, PCI-X option slots.
- A PCI, PCI-X expansion slot on the motherboard that is equipped for the 3.3V or 5V PCI signaling environment.
- PCI option cards used to create the local subsystem.
- An optional local processor to control the subsystem.

2.3 Software Requirements

The 31154 Bridge is shipped with the SROM programmed to the bridge's default register settings during module test. The 31154 Bridge may be used with a software utility that will allow the user to program the SROM to take advantage of the customers specific configuration requirements. Refer to the 31154 Bridge Component Specification for a complete description of the registers and their effects on the bridge.

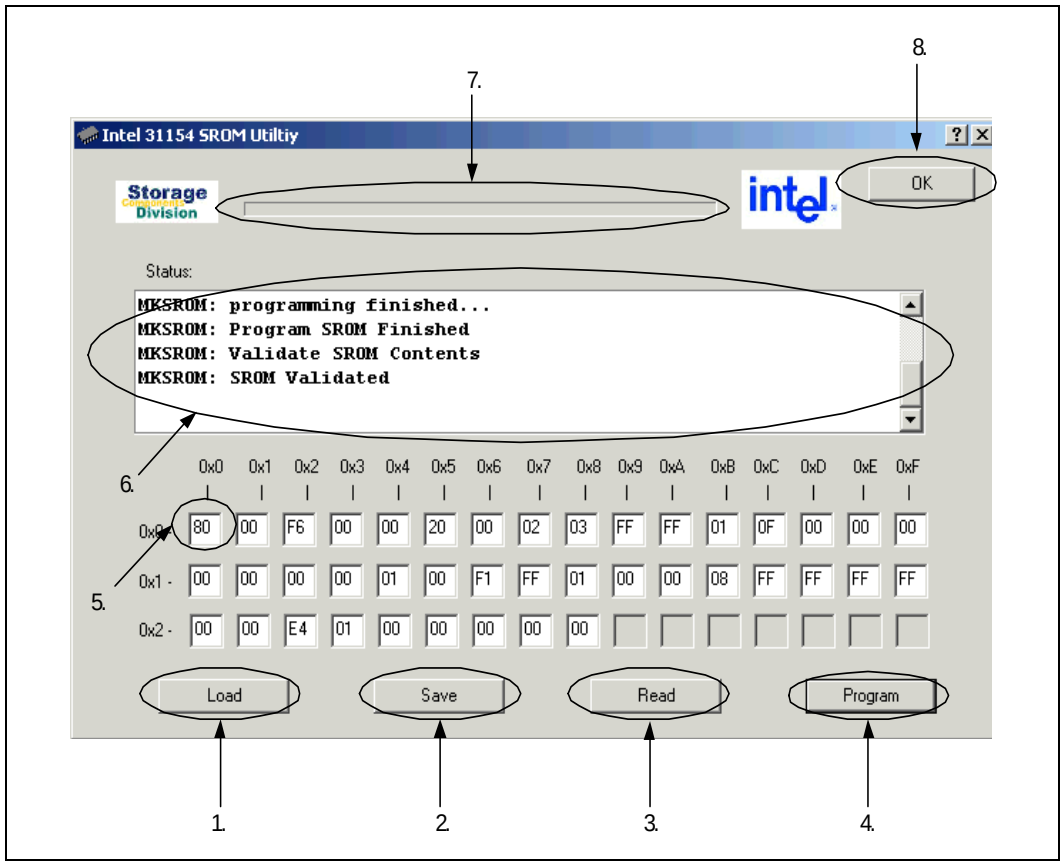
The 31154 SROM Utility ZIP file can be downloaded from the Intel Developers Web site. Use standard unzip procedures to install the program and associated files onto the system.

The utility must be loaded on a Microsoft Windows* 2000 platform or higher, as defined in Section 2.2. The 31154 Bridge must be installed in this system to allow access to the SROM.

2.3.1 Programming the SROM

It is possible to program the serial ROM on the 31154 Bridge using the 31154 SROM Utility. You can create a data file to load in the SROM by using any text editor.

Figure 2. 31154 Bridge SROM Utility Dialog Box



The SROM utility dialog box shown in Figure 2 has the following functions:

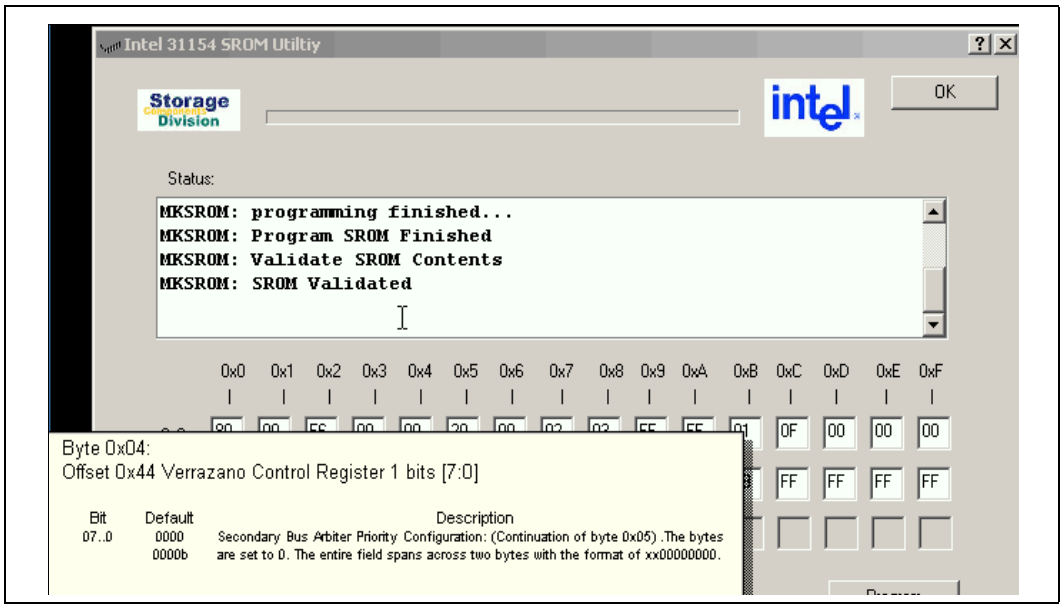
1. Selecting the Load button loads the SROM contents specified in a file to the screen. VzDefault.dat included in this distribution is a good example of a file that this utility will accept.
2. Selecting the Save button saves the contents on the screen to a file.
3. Selecting the Read button reads contents of the ROM to the screen.
4. Selecting the Program button allows you to program the ROM using the contents of the screen**.**
5. These are the bytes in the ROM that can be changed/updated. Each row equates to 16 bytes in the ROM.
6. Information Messages**.**
7. Status Bar**.**
8. OK button. Press this button to close the dialog box.

Note: Refer to the 31154 133MHz PCI Bridge Component Specification for byte definitions.

2.3.2 Help Button

The SROM utility supports contextual help. To access help, press the ? button in the upper right-hand corner of the dialog screen. Once selected, a question mark is added to the cursor. Move the cursor over the area in question and click the mouse. A description of the area will display. If you move the cursor over an individual byte, you will receive a brief definition of the contents of that byte.

Figure 3. SROM Help



Note: Under Microsoft Windows* 2000 or higher, you can cut and paste informational messages moving the mouse over them and right clicking the mouse.

2.4 Installation Procedure

Figure 1 on page 6 illustrates the 31154 Bridge and shows the location of components referred to in this section.

Install the 31154 Bridge as follows:

1. Power down the host system that will contain the 31154 Bridge.
2. Place the motherboard with the associated support devices on a bench if mechanical constraints do not allow testing of the 31154 Bridge and the expansion slots inside the system box.
3. Verify the DIP switch settings for J9, J20, and J21.
4. Configure your system as follows:
   a. Insert the card edge of the 31154 Bridge into a PCI, PCI-X slot.
   b. Insert a 3.3V, 5V or universal option PCI card into the PCI-X 100/66 MHz card slot J11 or the PCI-X 133 MHz card slot J2.
5. Power up the system.
6. Verify auto-configuration of the 31154 and of any devices that are plugged in as follows:
   a. If the on-board ROM is preloaded, the 31154 banner will be present.
   b. Verify that system BIOS or firmware detects and configures the 31154.
   c. To verify the loading of the SROM, run the 31154 SROM Utility without loading the 31154Default.dat file.
7. PCI bus data, address, and control signals are monitored by connecting a logic analyzer to MICTOR connectors U15, U16, and U17. (Refer to Table 10,Table 12, and Table 11)

Table 10. U15 MICTOR CONNECTOR, QS_AD<31:0>

Pin	Signal	Pin	Signal
1	NC	23	QS_AD23
2	NC	24	QS_AD7
3	NC	25	QS_AD22
4	NC	26	QS_AD6
5	NC	27	QS_AD21
6	NC	28	QS_AD5
7	QS_AD31	29	QS_AD20
8	QS_AD15	30	QS_AD4
9	QS_AD30	31	QS_AD19
10	QS_AD14	32	QS_AD3
11	QS_AD29	33	QS_AD18
12	QS_AD13	34	QS_AD2
13	QS_AD28	35	QS_AD17
14	QS_AD12	36	QS_AD1
15	QS_AD27	37	QS_AD16
16	QS_AD11	38	QS_AD0
17	QS_AD26	39	GND
18	QS_AD10	40	GND
19	QS_AD25	41	GND
20	QS_AD9	42	GND
21	QS_AD24	43	GND
22	QS_AD8		

Table 11. U16 MICTOR CONNECTOR, Command/Control

Pin	Signal	Pin	Signal
1	NC	23	S_GNT0REQ#
2	NC	24	QS_TRDY#
3	NC	25	S_GNT1#
4	NC	26	QS_IRDY#
5	NC	27	S_GNT2#
6	NC	28	QS_FRAME#
7	QS_C/BE2	29	S_GNT3#
8	QS_C/BE4	30	S_GNT8#
9	QS_C/BE3	31	S_GNT4#
10	QS_C/BE5	32	NC
11	NC	33	S_GNT5#
12	QS_C/BE6	34	NC
13	QS_SERR#	35	S_GNT6#
14	QS_C/BE7	36	QS_PAR64
15	QS_PERR#	37	S_GNT7#
16	QS_C/BE0	38	QS_PAR
17	QS_LOCK#	39	GND
18	QS_C/BE1	40	GND
19	QS_ACK64#	41	GND
20	QS_STOP#	42	GND
21	QS_REQ64#	43	GND
22	QS_DEVSEL#		

Table 12. U17 MICTOR CONNECTOR, QS_AD<63:32>

Pin	Signal	Pin	Signal
1	NC	23	QS_AD55
2	NC	24	QS_AD39
3	NC	25	QS_AD54
4	NC	26	QS_AD38
5	NC	27	QS_AD53
6	NC	28	QS_AD37
7	QS_AD63	29	QS_AD52
8	QS_AD47	30	QS_AD36
9	QS_AD62	31	QS_AD51
10	QS_AD46	32	QS_AD35
11	QS_AD61	33	QS_AD50
12	QS_AD45	34	QS_AD34
13	QS_AD60	35	QS_AD49
14	QS_AD44	36	QS_AD33
15	QS_AD59	37	QS_AD48
16	QS_AD43	38	QS_AD32
17	QS_AD58	39	GND
18	QS_AD42	40	GND
19	QS_AD57	41	GND
20	QS_AD41	42	GND
21	QS_AD56	43	GND
22	QS_AD40		

§ §